Signal Integrity

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Nanoroute: What is Signal and Power Integrity?

- **Signal Integrity ensures signals are of sufficient quality to reliably transmit their required information, and do not cause problems to themselves or to other components in the system.**
- **Signal Integrity applies to Digital, Analog and Power electronics**
- **Signal Integrity issues are more common now because electronics are more dense and chips have faster rise times**
  - **Assuring Signal Integrity now involves more knowledge of such RF techniques as terminations, impedance matching**
- **Major function of engineering, next to conceiving the correct design, is implementing the design correctly**
- **Signal integrity assures the circuit design operates as intended and must be designed in.**
  - **Correct design relies on experience, best practices, analysis and simulation to ensure desired signal quality.**

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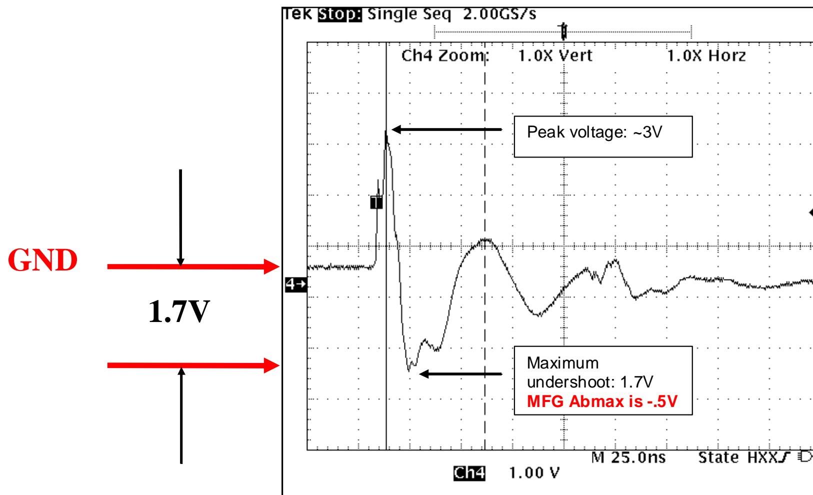
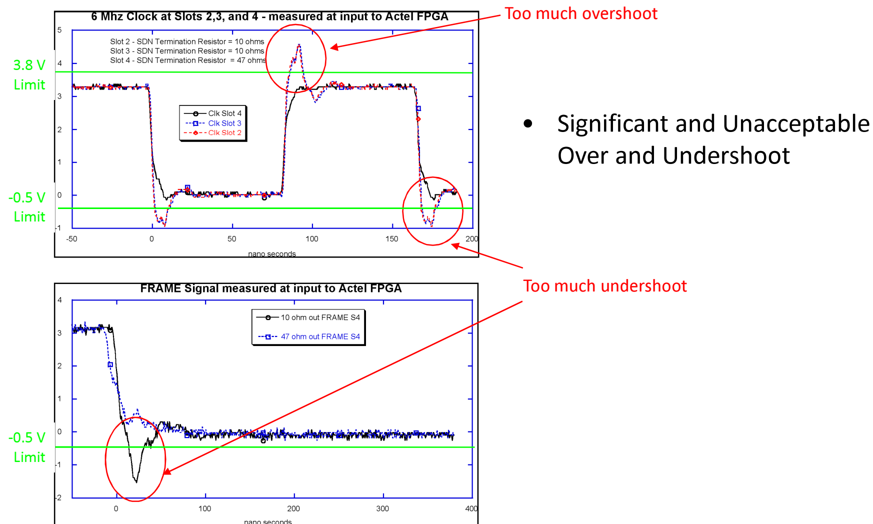
What is Signal and Power Integrity? (cont.)



What is Signal and Power Integrity? (cont.)



- Significant and Unacceptable Over and Undershoot

From: Ed James, GSFC, ACE Signal Integrity Tuning

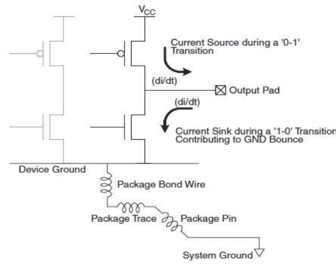
What is Signal and Power Integrity? (cont.)

Table 1 • SSO around a Quiet Output for SX-A, RT54SX-S, A500K, and ProASIC^{PLUS} Devices

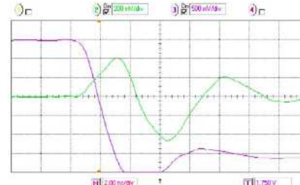
/O Voltage Compliance SSO	SSO	
	At High Slew	At Low Slew
SX-A/RTSX-S 5.0V	24*	>40*
SX-A/RTSX-S 3.3V	32**	>40**
ProASICPLUS 3.3V	32**	>40**
A500 3.3V	32**	>40**

Notes:

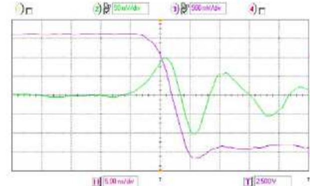
1. **The observed ground bounce is less than 1.5V with a pulse width of less than 2.0ns*
2. *** The observed ground bounce is less than 1.25V with a pulse width of less than 2.0ns*



- Is 1.5 or 1.25 volts of ground bounce OK?
- 1.5 volts almost 1/2 way between a logic "0" and "1" for 3.3 volt logic



High Slew
- Tfall = 1.5 ns
- Gnd Bounce = 0.4V



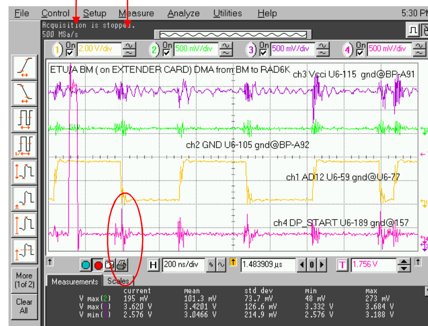
Low Slew
- Tfall = 6 ns
- Gnd Bounce = 0.1V

See: Actel SSO Signal Integrity. PDF, Simultaneously Switching Noise and Signal Integrity

What is Signal and Power Integrity? (cont.)

1) Valid "Start" Cycle Pulse (Red)

2) When Data Bits drive low (Yellow), ground bounces causing a phantom positive glitch on "Start" locking up the system



- Is every thing ok because the ambient "Functional Test" passed?

Purple - 3.3 V
0.5 V/div
Note more noise as AD driven "High"

Green - D Gnd
0.5 V/div
Note more noise as AD driven "Low"

Yellow - AD 12
2 V/div

Red – Start signal
0.5 V/div
Note signal is nominally driven "low", glitches represent internal chip ground

Designing the System Correctly

- Fundamentally, signal integrity must be designed in and not "discovered" by test.
  - Tests verify that signals have the intended integrity.
  - Tests are not designed to qualify a poor design
- Each designer identifies the critical signals and ensures their integrity is not compromised.
- Critical signals are supported by analysis, modeling, or technical rationale justifying why they are expected to work.
- Identified critical signals receive special layout attention assuring their proper functioning
- Signal Integrity analysis, test results, and scope pictures should be available at the final design review

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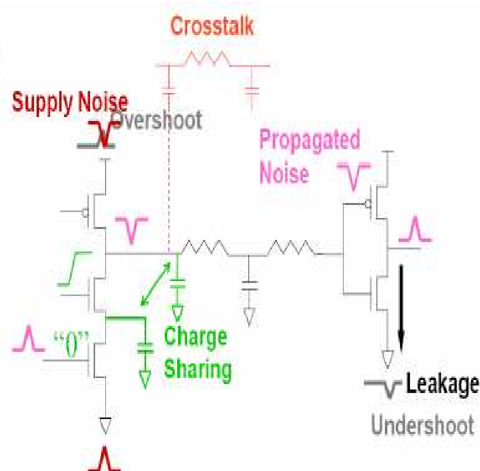
Signal integrity (SI) issue

✓ Signal Integrity (SI) Issue
- Crosstalk
- Charge sharing
- Supply noise
- Leakage
- Propagated noise
- Overshoot
- Under shoot



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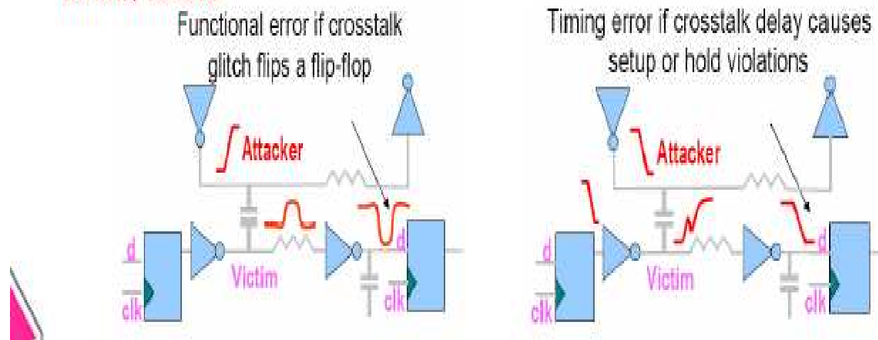
SI Closure

SI closure

- Occur when a design is free from SI induced functional glitch and timing failure



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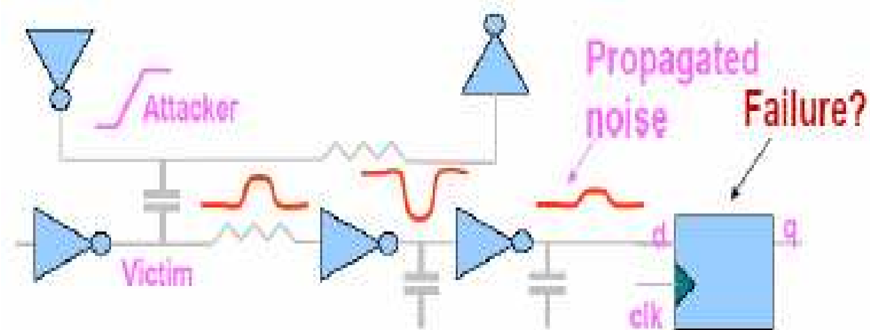
SI analysis



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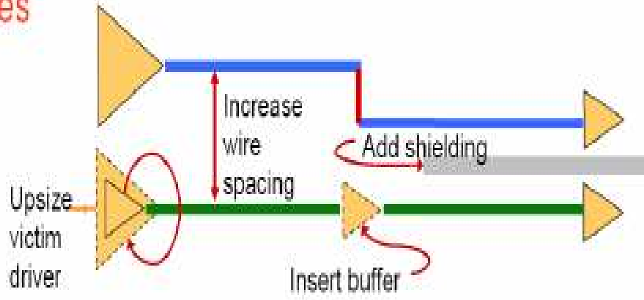
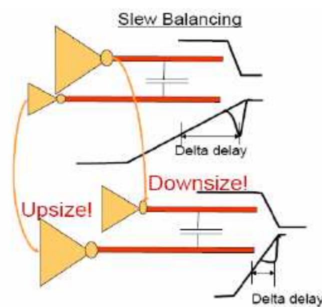
SI Prevention Techniques

SI repair techniques



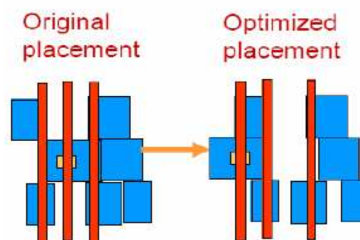
Signal Integrity Prevention 1

- **SI prevention**
  - Placement-based SI prevention
    - Reduce crosstalk glitch and delay variation
    - Reduce coupling capacitance



Original placement

Optimized placement

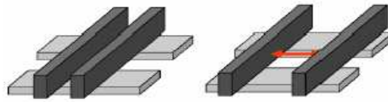


Signal Integrity Prevention 2

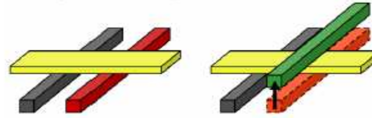
SI prevention (cont.)

– Routing-based SI prevention

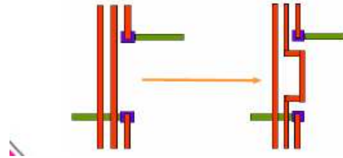
- Wiring Spacing



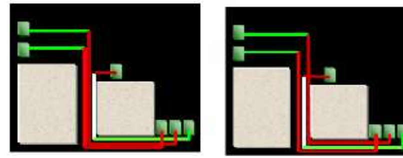
- Layer Switching



- Parallel Wires Reducing



- Net Re-ordering



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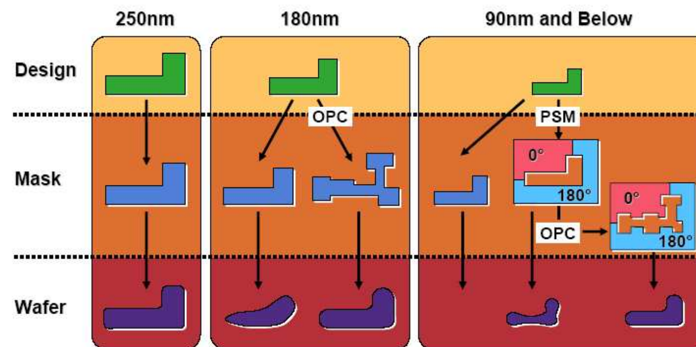
Mask producing



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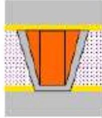
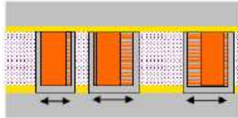
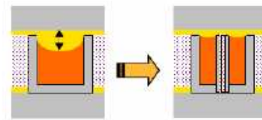
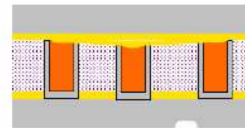
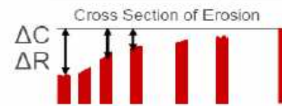
Conductors











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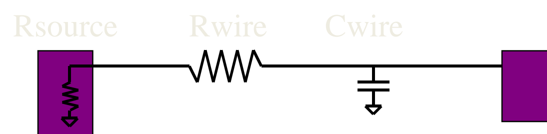
Crosstalk Prevention Strategies 1

- **Placement phase**
  - Don't know adjacencies, layer assignment, or global route
  - Do know net length, est. wire R/C, driver strength, signal slews
  - Metrics tell if a net is likely to have problems
  - Fixes (size driver, buffer signal) cause no convergence problems
- **Global route phase**
  - Don't know adjacencies, only congestion figure
  - Do know layer assignments, better R/C estimates



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Crosstalk Prevention Strategies

- Can apply timing windows
  - only consider signals that can change at the same time
  - data comes from static timing analysis
- Detailed routing - detailed analysis and routing ECOs
- N.B.: In any case, SI brings potential huge infrastructure changes (e.g., statistical centering design w/distributions)

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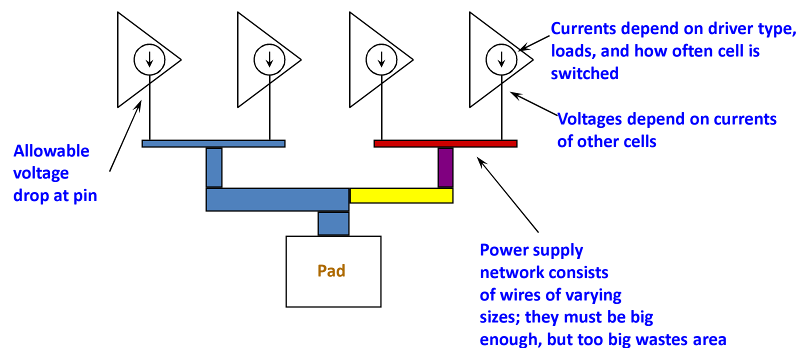
IR Drop

- Voltage drop in supply lines from currents drawn by cells
- Symptom: chip malfunctions on certain vectors
- Biggest problem: what's the worst-case vector?



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IR Drop

- Analysis
  - model I/O P/G supply; C extraction must distinguish decoupling cap between P/G and coupling cap between signals, P/G
- Prevention (good design)
  - P/G lines on same layer, close to each other; large decoupling on chip; process solutions (e.g., DEC Alpha)

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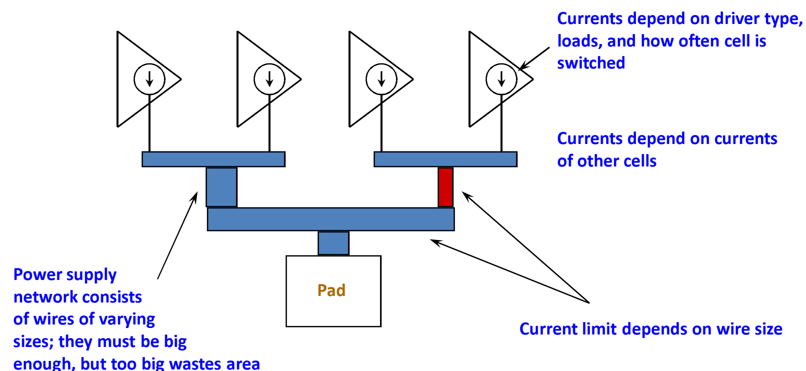
Electromigration

- **Power supply lines fail due to excessive current**
- **Symptom: chip eventually fails in the field when wire breaks**



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Electromigration

- Prevention: wire cross-section to current rules
- Maximum current density for particular material (via, layer)
- Modified Black's equation; waveform models
- Higher limits for short, thin wires due to grain effects
- Copper: 100x resistance to EM $\rightarrow$ not a problem any more? (actually, 4-5x)

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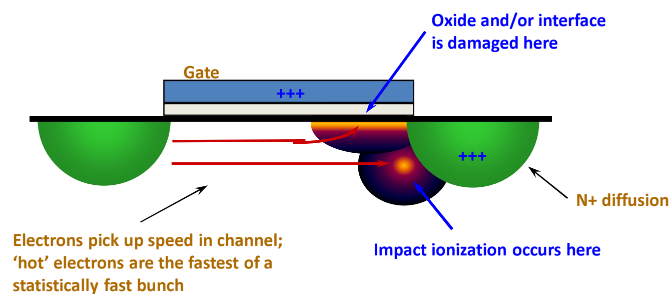
Hot Electron Effects

- May also be called short channel effect
- Caused by extremely high electric fields in the channel
  - Occurs when voltages are not scaled as fast as dimensions
- Effect becomes worse as devices are turned on harder
- Symptom: Thresholds shift over time until chip fails



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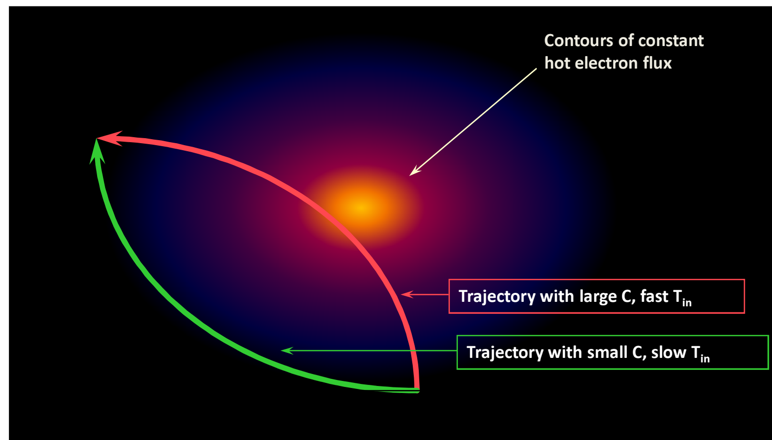
Hot Electron Effect (cont)

- Depends on how hard device is driven (input slew rate)
- And on the size of the load



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Hot Electron Prevention Strategies

- **Allowable region for input slew and output load**
- **Fluence per transition is function of input slew, output load**
- **Set maximum allowed degradation over life of device (estimate of total number of transitions) ≡ fluence limit**
- **Size device as needed**
- **Output load vs. driver sizes**

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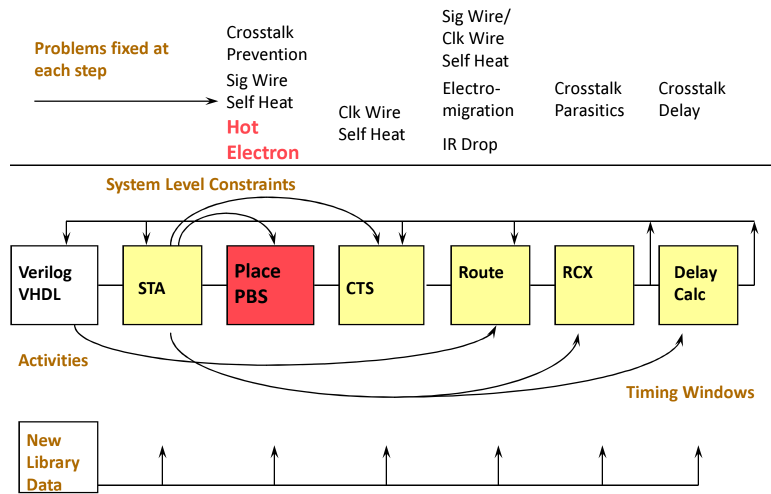
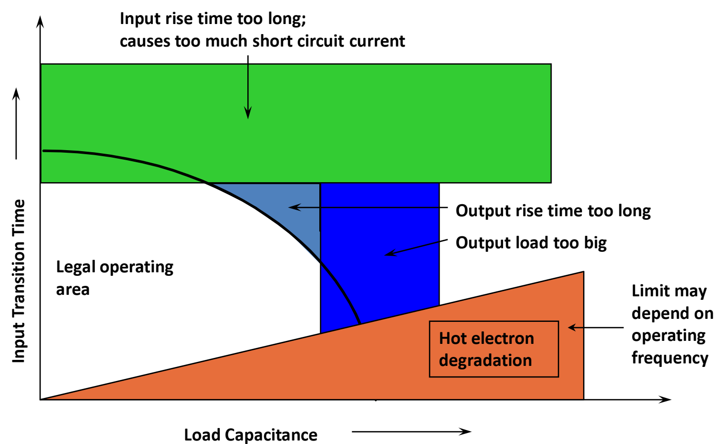
SI Flow - Hot Electron

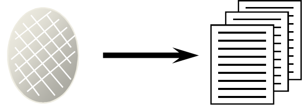


New Design Rule for Hot Electron Effects

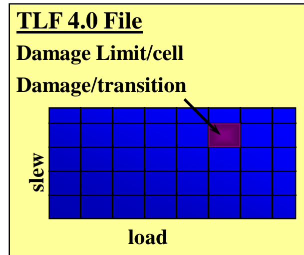
- Allowable region for input slew and output load



Hot Electron Characterization



- Get raw process degradation
- Select cell EOL performance (5% timing loss over life)



- Use BTA BERT model to compute total acceptable fluence
- Compute fluence per transition as a function(load, slew)
- Compute Total fluence

Total fluence = fluence/transition * freq * lifetime

- Replace Driver, as needed

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Wire Self-Heat

- **May also be called signal wire electromigration**
- **Wire heats above oxide temperature as pulses go through**
- **Symptom: chip eventually fails when wire breaks**
- **Depends on metal composition, signal frequency, wire sizes, slew rates, and amount of capacitance driven**
- **Requires different data/formulas from power supply EM**

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